REMARKS

This amendment responds to the Office Action dated October 24, 2002, in which the Examiner rejected claims 1, 7, 8, 15, 17 and 18 under 35 U.S.C. §102(e), rejected claims 9, 19 and 20 under 35 U.S.C. §103 and objected to claims 2-6, 10-14 and 16 as being dependent upon a rejected base claim but would be allowable if rewritten in independent form.

As indicated above, claim 1 has been cancelled without prejudice and objected to claims 2 and 10 have been rewritten into independent form. Therefore, Applicant respectfully requests the Examiner withdraws the objection to claims 2-6 and 10-14 and withdraws the rejection to claims 7-8 under 35 U.S.C. §102(e) and claim 9 under 35 U.S.C. §103.

Claim 15 claims a circuit modification method of modifying a circuit by inserting one or more buffers into a predetermined wire located within the circuit. The method comprises the steps of: first, determining whether a glitch error is caused in the predetermined wire by an aggressor comprised of one or more other wires. When a glitch error is caused in the predetermined wire by an aggressor, determining a number of buffers to be inserted into the predetermined wire based on an amount of glitch to be caused in the predetermined wire by the aggressor.

Through the method of the claimed invention determining a number of buffers to be inserted based upon an amount of glitch, as claimed in claim 15, the claimed invention provides a circuit modification method capable of eliminating glitch errors. The prior art does not show, teach or suggest the method as claimed in claim 15.

Claims 20 claims a circuit modification method comprising the steps of: first, determining whether a glitch error is caused in the predetermined wire by an aggressor comprised of one or more other wires. When a glitch error is caused in the predetermined wire by an aggressor, replacing a driving circuit for driving the predetermined wire with another one having a higher driving ability than the driving circuit.

Through the method of the claimed invention replacing a driving circuit with another one having a higher driving ability, as claimed in claim 20, the claimed invention provides a circuit modification method which decreases the amount of glitch. The prior art does not show, teach or suggest the invention as claimed in claim 20.

Claims 15, 17 and 18 were rejected under 35 U.S.C. §102(e) as being anticipated by *Alpert et al.* (U.S. Patent No. 6,117,182).

Applicant respectfully traverses the Examiner's rejection of the claims under 35 U.S.C. §102(e). The claims have been reviewed in light of the Office Action, and for reasons which will be set forth below, Applicant respectfully requests that the Examiner withdraws the rejection to the claims and allows the claims to issue.

Alpert et al. appears to disclose in Fig. 3a an integrated circuit environment having a victim net 52. A net is comprised of at least one source node 56, and at least one sink or receiving node 58 and a conductor or transmission line 12. Aggressor net 53 conducts a aggressor pulse 54. A corresponding noise pulse 60 is induced into victim net 52 due to coupling capacitance 66 between aggressor net 53 and victim net 52. The amount of coupling capacitance from aggressor net 53 to victim net 52 is proportional to the distance that aggressor net 53 and victim net 52 run parallel to each other on an integrated circuit. If the

level of 1st noise pulse 60 exceeds a switching threshold level of a coupled device such as receiving node 58, unintentional switching of the coupled device may result. Unintentional switching can cause serious consequences such as chip malfunction. Referring to FIG. 3b, buffer 68 has been inserted in transmission line 12 a calculated distance 65 from receiving node 58 to reduce the level of 1st noise pulse 60 of FIG. 3a to the level of 2nd noise pulse 61 of FIG. 3b. Like parts are identified by like reference numerals in FIGS. 3a and 3b. The intensity of 2nd noise pulse 61 is inconsequential as long as it does not exceed the switching threshold level of buffer 68. Inserting buffer 68 into victim net 52 suppresses 2nd noise pulse 61. Aggressor pulse 54 and corresponding 2nd noise pulse 61 and 3rd noise pulse 62 illustrate the noise effects that the aggressor net 53 has on the victim net 52 with buffer 68 inserted. In the absence of buffer 68, 2nd noise pulse 61 and 3rd noise pulse 62 would, in effect, combine to form a larger pulse such as 1st noise pulse 60 from FIG. 3a which exceeds the switching threshold level of receiving node 58 and a device coupled to receiving node 58 could erroneously switch to an ON state. (col. 6, line 51 through col. 7, line 16) Corresponding to the step indicated at reference numeral 83 of FIG. 5, if a noise level is calculated which is less than the allowable noise margin, no buffer insertion is required and the method returns to calculate on a new interconnect segment. However, if the calculated noise exceeds the noise margin, an optimum location for buffer placement with reference to the sink is determined in the step indicated at reference numeral 85. Each source node to sink node conductor having a noise violation requires a determination of the optimum length for buffer insertion. This is determined utilizing the step indicated at reference numeral 85. R is the conductor resistance per unit length $R=R_e/l_e$ and $I=I_e/l_e$, I is the current per unit length. (col. 11, line 66 through

col. 12, line 13) The maximum conductor length allowable for equation 7 is achieved when the buffer resistance and downstream current are zero. Setting the buffer resistance and the downstream current to zero, yields a conductor length of 2NS(v)/(IR). A maximum conductor length approximation is useful for noise avoidance when a driver's properties are unknown or if the ratio of the buffer's resistance to conductor resistance is very small. Referring to equation 7, the ratio λ_j of coupling capacitance or "bad capacitance" to total capacitance is inversely proportional to the distance d separating the aggressor and victim nets, i.e., $\lambda_j = k_j / d$, for a defined constant k_j. (col. 12, lines 44-56) In summary, at a given node, equation 5 is utilized to determine if adding a buffer is necessary. Then the method computes compliance by inserting a buffer at a furthest possible location from the destination (sink) of the signal. Each transmission line from node to node is checked. The method terminates when the signal source node is reached. (col. 13, lines 24-29)

Thus, *Alpert et al.* merely discloses at column 12, lines 45-50 determining the conductor length for buffer insertion based upon noise slack NS, current I and conductor resistance R. Nothing in *Alpert et al.* shows, teaches or suggests determining the number of buffers based upon an amount of glitch as claimed in claim 15. Rather, *Alpert et al.* merely discloses determining the maximum conductor length based upon noise slack, current and resistance.

Also, *Alpert et al.* merely discloses at column 11, lines 67 through column 12 line 6 determining if a noise exceeds a noise margin to determine if buffer insertion is required. Nothing in *Alpert et al.* shows, teaches or suggests determining the number of buffers to be

inserted based upon an amount of glitch as claimed in claim 15. Rather, *Alpert et al.* merely discloses using noise level to determine whether placement is required.

Since nothing in *Alpert et al.* shows, teaches or suggests determining the number of buffers to be inserted based upon an amount of glitch as claimed in claim 15, it is respectfully requested that the Examiner withdraws the rejection to claim 15 under 35 U.S.C. §102(e).

Claims 17 and 18 depend from claim 15 and recite additional features. It is respectfully submitted that claims 17 and 18 would not have been anticipated within the meaning of 35 U.S.C. §102(e) by *Alpert et al.* at least for the reasons as set forth above.. Therefore, it is respectfully requested that the Examiner withdraws the rejection to claims 17 and 18 under 35 U.S.C. §102(e).

Claims 19 and 20 were rejected under 35 U.S.C. §103 as be unpatentable over *Alpert et al.* in view of *Huang* (U.S. Patent No. 5,568,395).

Applicant respectfully traverses the Examiner's rejection of the claims under 35 U.S.C. §103. The claims have been reviewed in light of the Office Action, and for reasons which will be set forth below, applicant respectfully requests that the Examiner withdraws the rejection to the claims and allows the claims to issue.

As discussed above, *Alpert et al.* merely discloses determining buffer placement based upon a noise level not exceeding an allowable noise margin. Nothing in *Alpert et al.* shows, teaches or suggests replacing a driving circuit with another one having a higher driving ability as claimed in claim 20. Rather, *Alpert et al.* merely discloses determining if

a buffer should be inserted based upon a calculated noise level being greater than an allowable noise margin.

Huang appears to disclose a system for modeling and estimating crosstalk noise and detecting false logic. The noise is caused by culprit signal nets that are in a switching state and affect a victim net which is in a non-switching (DC) steady state. This estimated noise is evaluated to determine whether any false logic results in the victim net. (col. 1, lines 36-40) Crosstalk system 120, an executable application running on processing unit 102 as shown in FIG. 1, utilizes information from the foregoing applications to estimate crosstalk noise on select signal nets based on a model described below. Should this estimated noise be sufficiently large, a false logic is detected and the circuit design is returned to layout planner 116 to reroute the subject signal nets in order to eliminate the noise. (col. 5, lines 18-25)

Thus, *Huang* merely discloses rerouting signal nets if a false logic is detected. Nothing in *Huang* shows, teaches or suggests replacing a driving circuit with another one having a higher driving ability as claimed in claim 20. Rather, *Huang* merely discloses rerouting to eliminate noise.

The combination of *Alpert et al.* and *Huang* would merely suggest to insert a buffer if a calculated noise level is greater than an allowable noise margin as taught by *Alpert et al.* and to reroute the subject signal to eliminate noise if a false logic is detected as taught by *Huang*. Thus nothing in the combination show, teaches or suggests replacing a driving circuit with another one having a higher driving ability as claimed in claim 20. Therefore,

it is respectfully requested that the Examiner withdraws the rejection to claim 20 under 35 U.S.C. §103.

Claim 19 recites additional features. It is respectfully submitted that claim 19 would not have been obvious within the meaning of 35 U.S.C. §103 over *Alpert et al.* and *Huang* at least for the reasons as set forth above. Therefore, it is respectfully requested that the Examiner withdraws the rejection to claim 19 under 35 U.S.C. §103.

Since objected to claim 16 depend from an allowable claim, it is respectfully requested that the Examiner withdraws the objection thereto.

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason Examiner feels that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, applicant respectfully petitions for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

By: _____
Ellen Marcie Emas
Registration No. 32,131

P.O. Box 1404
Alexandria, Virginia 22313-1404
(703) 836-6620

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Attachment to Amendment dated January 21, 2003

Marked-up Claims 2, 7, 9 and 10

2. (Amended) [The] A circuit modification method of modifying a circuit by inserting one or more buffers into a predetermined wire located within the circuit, the method comprising the steps of:

determining whether a glitch error is caused in said predetermined wire by one or more aggressors each comprised of one or more other wires;

when determining that a glitch error is caused in said predetermined wire by one or more aggressors, determining one or more positions where one or more buffers are to be inserted into said predetermined wire based on a coupling capacity between each of said one or more aggressors and said predetermined wire, [according to Claim 1,] wherein said insertion position determining step includes the steps of, when determining that a glitch error is caused in said predetermined wire by only one aggressor, calculating a target coupling capacity using the coupling capacity between said aggressor and said predetermined wire, and, when dividing said predetermined wire into a plurality of wire segments, determining one or more internal points of division of said predetermined wire so that a coupling capacity between each of said plurality of wire segments and said aggressor does not exceed said target coupling capacity, and setting said one or more internal points of division to said one or more positions where said one or more buffers are to be inserted into said predetermined wire.

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Marked-up Claims 2, 7, 9 and 10

7. (Amended) The circuit modification method according to Claim [1] 2, wherein said one or more buffers to be inserted into said predetermined wire have a driving ability equal to or greater than that of a driving circuit for driving said predetermined wire.

9. (Amended) The circuit modification method according to Claim [1] 2, further comprising the steps of, when determining that a glitch error is caused in said predetermined wire by one or more aggressors, replacing a driving circuit for driving said predetermined wire with another one having a higher driving ability than the driving circuit, and, before performing said insertion position determining step, determining whether a glitch error is caused in said predetermined wire driven by the other driving circuit by said one or more aggressors.

10. (Amended) [The] A circuit modification method of modifying a circuit by inserting one or more buffers into a predetermined wire located within the circuit, the method comprising the steps of:

determining whether a glitch error is caused in said predetermined wire by one or more aggressors each comprised of one or more other wires;

when determining that a glitch error is caused in said predetermined wire by one or more aggressors, determining one or more positions where one or more buffers are to be inserted into said predetermined wire based on a coupling capacity between each of said one

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Marked-up Claims 2, 7, 9 and 10

or more aggressors and said predetermined wire, [according to Claim 1,] wherein said insertion position determining step includes the steps of, when determining that a glitch error is caused in said predetermined wire by a plurality of aggressors, calculating a plurality of target coupling capacities respectively associated with said plurality of aggressors by using the coupling capacity between each of said plurality of aggressors and said predetermined wire, and, when diving said predetermined wire into a plurality of wire segments, determining one or more internal points of division of said predetermined wire so that a coupling capacity between each of said plurality of wire segments and each of said plurality of aggressors does not exceed a corresponding one of said plurality of target coupling capacities, and setting said one or more internal points of division to said one or more positions where said one or more buffers are to be inserted into said predetermined wire.